

REMARKS

I. Introduction

Claims 16 to 28 are pending in the present application. In view of the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

II. Rejection of Claims 16 to 20, 23, and 24 Under 35 U.S.C. § 102(b)

Claims 16 to 20, 23, and 24 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,604,380 (“Nishimura et al.”). It is respectfully submitted that Nishimura et al. do not anticipate these claims for at least the following reasons.

Claim 16 relates to a layer system and recites a an etching layer, whereby the etching layer is a silicon layer, and ***a passivation layer applied at least regionally to a surface of the silicon layer***, wherein the passivation layer includes a first, at least largely, inorganic partial layer and a second partial layer, and the second partial layer is made of an organic compound.

Nishimura et al. relate to a semiconductor device having a multilayer interconnection structure and disclose, referring to Figure 2(d), a silicon semiconductor substrate 1, an insulating film 2 formed on the substrate 1, a wiring layer 3 formed on the insulating film 2, a silicon oxide film 4 covering the wiring layer 3, a resin film 5 formed on the silicon oxide film 4, a silicon oxide film 6 formed on the resin film 5, and a second wiring layer 7 formed on the silicon oxide film 6. See col. 9, lines 54 to 64. In formulating the present rejection, the Office Action contends at page 3, referring to Nishimura et al., that the substrate 1 is an etching layer and the resin film 5 and the silicon oxide film 4 and/or the silicon oxide film 6 constitute a passivation layer. Applicants respectfully disagree. It is initially noted that components 4, 5, and/or 6 do not constitute a passivation layer. Notwithstanding the foregoing, the ***substrate 1***, relied upon as purportedly disclosing an etching layer, ***is separated from the resin film 5 and the silicon oxide films 4 and/or 6 by the insulating film 2***. As such, these components 4, 5, and 6 are ***not applied at least regionally to a surface of a silicon etching layer***, as recited in claim 16.

As indicated above, Nishimura et al. do not disclose, or even suggest, all of the features recited in claim 16. As such, it is respectfully submitted that Nishimura et al. do not anticipate claim 16.

Claims 17 to 20, 23, and 24 depend from claim 16 and therefore include all of the features recited in claim 16. Accordingly, it is respectfully submitted that Nishimura et al. do not anticipate these dependent claims for at least the same reasons set forth above in support of the patentability of claim 16.

In view of the foregoing, withdrawal of this rejection is respectfully requested.

III. Rejection of Claims 21, 22, and 25 to 28 Under 35 U.S.C. § 103(a)

Claims 21, 22, and 25 to 28 were rejected under 35 U.S.C. § 103(a) as unpatentable over Nishimura et al. It is respectfully submitted that Nishimura et al. do not render unpatentable these claims for at least the following reasons.

Claims 21, 22, and 25 to 28 depend from claim 16 and therefore include all of the features recited in claim 16. As more fully set forth above, Nishimura et al. do not disclose, or even suggest, all of the features recited in claim 16. As such, it is respectfully submitted that Nishimura et al. do not render unpatentable these dependent claims for at least the same reasons more fully set forth above in support of the patentability of claim 16. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Conclusion

In light of the foregoing, it is respectfully submitted that all of the presently pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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